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Enhancing Speed and Efficiency for High Transient Automotive Applications

Jon Wallace, Senior Director,
Issac Siavashani, Principal Engineer, and
Alexandr Ikriannikov, Fellow

Abstract

As ADAS and other high current applications are proliferating in automotive applications, the computing power of the related GPUs and ASICs continues to rise significantly. This puts additional pressure on the performance of voltage regulators for such demanding loads, where the currents increase and transients become larger and faster. Efficiency expectations continue to grow at the same time, while the load voltages decrease below 1 V for better thermal management and to enable advanced semiconductor processes with faster clocks. As low load voltage proportionally slows down the unloading transient and therefore causes a large increase in the bypassing capacitance, the voltage tolerance and transient specs are also tightening. This calls for smaller and faster inductances in the multiphase voltage regulator to support such aggressive transients. The question is where patented ADI coupled inductors can support the fastest current slew rates, while simultaneously minimizing the current ripple and supporting high efficiency in a small solution size.

Introduction

High current, low voltage applications frequently employ a multiphase buck converter topology for the voltage step down. This multiphase buck can utilize traditional discrete inductors (DL), as shown in Figure 1a, or coupled inductors (CL), as depicted in Figure 1b. In the case of CL, the windings are magnetically coupled, providing the advantage of current ripple cancellation.[1-6]

Automotive ADAS applications face a challenge in maintaining tight regulation for GPU or ASIC rails within the 0.4 V to 1 V range, especially under fast transient conditions. A loading transient generally causes all phases to turn the switching nodes V_X high to V_{IN}, so the inductor current in each phase ramps up with a slew rate (1), where V_{IN} is input voltage, V_o is output voltage, and L is inductance value. An unloading transient typically causes all phases to turn low to GND and the inductor current ramps down (2). Given the low output voltage value V_{OUT} < 1 V and assuming that the input voltage is typically 5 V or even higher, it is easy to see from the comparison of equations 1 and 2 that the unloading transient creates the main problem as there is only a small voltage to ramp the current down.

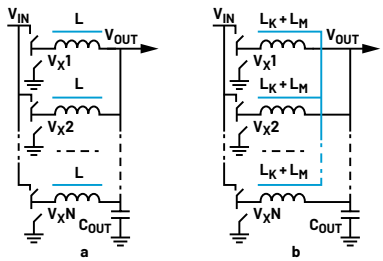

Figure 1. Multiphase buck converter with (a) discrete inductors and (b) coupled inductors.

$$\frac{dIL_{UP}}{dt} = \frac{V_{IN} - V_O}{L} \quad (1)$$

$$\frac{dIL_{DOWN}}{dt} = \frac{-V_O}{L} \quad (2)$$

The simple solution involves increasing the number of ceramic output capacitors in C_{OUT}. However, the size and cost of this approach can swiftly become impractical. In the automotive industry, voltage regulators are often configured to switch at a relatively higher frequency (F_S), typically exceeding 2 MHz. This is in contrast to regulators in cloud or industrial applications. The higher switching frequency is necessary in automotive settings due to specific electromagnetic interference (EMI) requirements. While this choice helps to decrease inductance values in the regulator, further enhancements are still required.

The current ripple in each phase of the conventional buck with DL can be found as Equation 3, where the duty cycle is $D = V_{OUT}/V_{IN}$, V_{OUT} is the output voltage, V_{IN} is the input voltage, L is inductance value, and F_S is the switching frequency.

$$dIL_{DL} = \frac{V_{IN} - V_O}{L} \times \frac{D}{F_S} \quad (3)$$

Replacing the DL with CL that has a leakage inductance L_K and the mutual inductance L_M, the current ripple in CL can be shown as Equation 4.[6] The term defined as figure of merit (FOM) is expressed as Equation 5, where N_{PH} is the number of coupled phases, ρ is a coupling coefficient (Equation 6), and j is a running

index, which just defines an applicable interval of the duty cycle (Equation 7). The parameters of the CL are the leakage inductance L_K and the mutual inductance L_M.

$$dIL_{CL} = \frac{V_{IN} - V_{OUT}}{L_K} \times \frac{D}{F_S} \times \frac{1}{FOM_{CL}(D, N_{PH}, \rho, k)} \quad (4)$$

$$FOM_{CL} = \frac{\left(1 + \frac{\rho}{\rho+1} \times \frac{1}{N_{PH}-1}\right)}{1 - \left[\frac{(N_{PH}-2\times j-2) + \frac{j\times(j+1)}{N_{PH}\times D}}{+\frac{N_{PH}\times D\times(N_{PH}-2\times j-1)+j\times(j+1)}{N_{PH}\times(1-D)}}\right] \times \frac{\frac{\rho}{\rho+1}}{N_{PH}-1}} \quad (5)$$

$$\rho = \frac{L_M}{L_K} \quad (6)$$

$$j = floor(D \times N_{PH}) \quad (7)$$

The meaning of FOM in equations 4 and 5 for the particular CL design can be interpreted as an additional multiplier in current ripple cancellation as compared to the conventional buck with discrete inductor L. The definition of FOM and its meaning were also generalized and extended[11] to compare any systems with arbitrary current ripple and transient performances. The proposal is to use a ratio of the normalized transient spew rate (desired high) to the normalized current ripple (desired low) (Equation 8). The transient slew rate and the current ripple are normalized by related numbers for some benchmark converters with discrete inductors (so any system with DL will still lead to FOM = 1). The SR_{TR} and ΔIL are transient current slew rate and current ripple in a steady state of the chosen design or technology, while SR_{TR_DL} and ΔIL_{DL} are the same parameters but for the benchmark DL design.

Equation 8 can be simplified into Equation 9, using the fact that the current slew rate for the discrete inductor is the same in transient and steady state. This way, any actual reference to DL design is completely removed, while the benchmarking ideology is still there.

$$FOM = \frac{SR_{TR}}{SR_{TR\_DL}} \Big/ \frac{\Delta IL}{\Delta IL_{DL}} \quad (8)$$

$$FOM = \frac{SR_{TR}}{\Delta IL} \times D \times T_S \quad (9)$$

Notice that using the generalized FOM definition, Equation 9, for the CL will result in Equation 5, so the new definition is backward compatible, but can also be used for technologies where both current ripple and transient slew rate are arbitrarily different from the DL equations (for example, TLVR[9]).

CL Design and Considerations

The application specifications are V_{IN} = 5 V, V_{OUT} = 0.8 V, F_S = 2.1 MHz, and N_{PH} = 8. As a starting point, DL = 32 nH is chosen to support the fast transient, while each inductor occupies 4.2 mm × 4.2 mm × 4.2 mm. Ideally, these would be substituted with an 8-phase coupled inductor (CL). However, the low height requirement of h = 4 mm presents a challenge, as it would make such a lengthy component unmanufacturable due to being excessively thin and long, while also increasing sensitivity to board flex. Therefore, the 4-phase building block was chosen for CL. This also enables better flexibility with placement and layout. As the faster transient is targeted and knowing that the CL will have smaller ripple than the starting DL value, the recently introduced Notch CL (NCL) structure was proposed to minimize the leakage value L_K.[7,8,10] The NCL0804 was designed with L_K~17 nH and OCL = L_M + L_K = 100 nH, N_{PH} = 4, phase pitch 6.9 mm/phase, and a height h = 4.0 mm max (Figure 2).

Figure 2. Developed NCL0804-4-R17 (h = 4 mm max).

A good way to compare different designs is a FOM plot.[10] Any DL design will have FOM = 1, as the trade-off between the current slew rates in steady state and transient is 1:1. The NCL structure of the coupled inductor maximizes L_M/L_K ratio in a given size, so it generally results in the highest FOM.[9] The FOM comparison is shown in Figure 3, where the developed NCL is ~4.4× better than DL around the targeted output voltage.

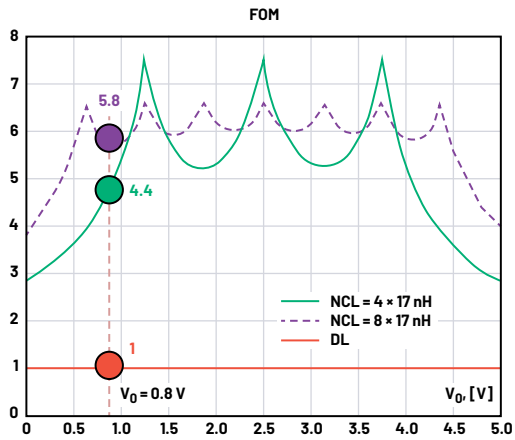

Figure 3. FOM for the developed NCL = 4× 17 nH and theoretical NCL = 8× 17 nH as a function of the output voltage V_{OUT} compared to the FOM of any DL (V_{IN} = 5 V).

Table 1. Comparison of the Different Magnetics Options for the Four-Phase Building Block

Inductor	Height: mm/Relative	Efficiency, Relative	Current Ripple, Relative	Transient, Relative	Relative Transient/Ripple Benefit (Equation 9)[11]
NCL0804-4	4.0 max/1×	OK	1×	1×	4.4×
DL = 32 nH	4.4 max/1.1× larger	Low	2.35× larger	1.9× slower	1×
DL = 100 nH	6.4 max/1.6× larger	OK	1.33× smaller	5.9× slower	1×

The corresponding current ripple comparison is shown in Figure 4 and Table 1. While the DL value can be chosen in a wide range for a different compromise between current ripple and transient slew rate, the advantage of developed NCL is always 4.4×. This correlates to 2.35× smaller current ripple than the ripple of DL = 32 nH while NCL is 1.88× faster. Then 2.35 × 1.88~4.4, matching the predicted FOM = 4.4. The current ripple can also be lowered a lot by using DL = 100 nH, which makes it 1.33× smaller current ripple than that in NCL, but NCL is then 5.88× faster, resulting in the same 5.88/1.33~4.4× advantage of NCL over any DL (FOM = 4.4 for NCL).

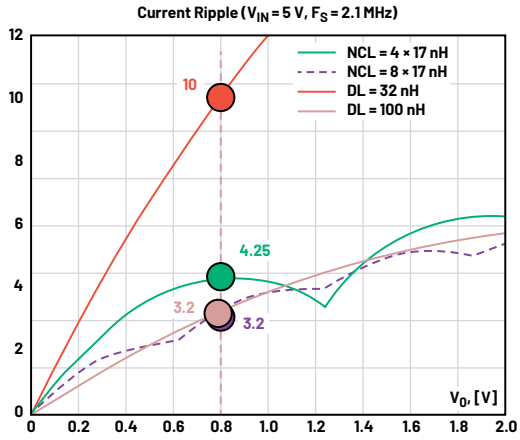

Figure 4. Current ripple for the developed NCL=4× 17 nH and theoretical NCL = 8× 17 nH compared to DL = 32 nH and DL = 100 nH as a function of the output voltage V_{OUT}.

Looking at a theoretical FOM for the same NCL in Figure 3 but considering if N_{PH} = 8 is manufacturable: the performance advantage of NCL over DL would increase from 4.4× to 5.8×, and make even more relative difference at a lower V_{OUT}.

Looking ahead, it might be worth considering a different design for the NCL. One possibility is arranging the phases in two rows to maintain a low aspect ratio (length/height) of the ferrite core, making it conducive to manufacturing. In this scenario, the NCL could potentially be positioned at the bottom of the PCB, directly above the ceramic bypass for the GPU, with power stages surrounding the NCL on the perimeter. The approach, akin to a vertical power delivery (VPD) arrangement, could potentially enhance the trade-off between transient and ripple (effectively transient efficiency). However, it's crucial to note that implementing such a change would be a significant departure from the existing design and layout. Whether this proposed approach is considered in the future will depend on customer preferences.

Experimental Results

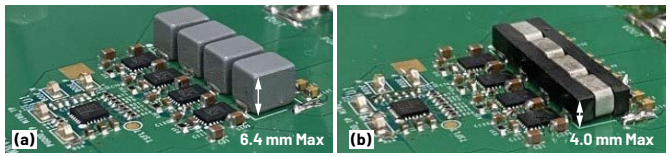

Figure 5. The voltage regulator four-phase building block with inductor footprint that accepts (a) DL = 100 nH (h = 6.4 mm max) and (b) NCL0804-4 (h = 4.0 mm max).

Substituting the DL = 32 H inductors with NCL0804-4 resulted in enhanced efficiency, as shown in Figure 6. This improvement is mainly attributed to the significant reduction in current ripple (Figure 4), leading to lower rms currents in windings, power stages, and traces. Additionally, it contributes to lower AC losses, as depicted in Figure 6. At the same time, the 17 nH/phase NCL (Figure 5b) offers ~1.9× faster current slew rate in transient and generally improves the phase margin in the feedback loop. Stepping down on ripple with DL = 100 nH (Figure 5a) recovers the efficiency, Figure 6, but such DL is significantly taller than the allowed h = 4 mm height, while also being ~5.9× slower than developed NCL. The latter would cause extreme implications for the amount of needed output capacitors. The results confirm the fundamental performance advantage of NCL as expected from the FOM estimates, against the different trade-off options of the discrete inductor approach.

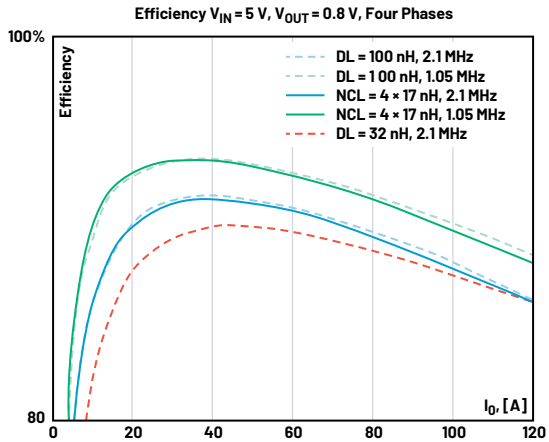

Figure 6. Efficiency comparison of the DL = 32 nH (h = 4.4 mm), DL = 100 nH (h = 6.4 mm), and NCL = 4× 17 nH (h = 4.0 mm): 5 V to 0.8 V, four phases.

Conclusion

In summary, a new coupled inductor with the NCL structure was developed to optimize performance for an application with very low output voltage and aggressive load transient specifications. This CL was also done to fit the specified low profile for the automotive design. The NCL structure was chosen to minimize leakage, achieving a formal benefit of over 4× in transient/ripple performance compared to the conventional discrete inductor option.

To match the efficiency of the developed NCL, a discrete inductor (DL) with 1.6× the height (DL = 100 nH) would be needed. However, this alternative would fall 5.9× behind in transient speed, significantly impacting the size and cost of the output capacitance. The comparison in Table 1 highlights the advantages of the NCL0804-4 in terms of height, efficiency, current ripple, and transient speed.

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About the Authors

Jon Wallace received his B.S. degree in computer and electrical engineering from Purdue University. Jon has been working in the automotive industry for 30 years. Prior to joining Analog Devices, Jon worked for 11 years as a software and hardware engineer at TRW Automotive, Inc. developing hardware and software for safety electronics. In 2005, he joined Maxim (now part of ADI) as a product definer for automotive power and related products. He has 25 issued U.S. patents in the fields of vehicle bus communications and software algorithms. The revenue for his defined products has exceeded $800M to date.

Issac Siavashani is a senior application engineer for the Automotive Business Team at Analog Devices. He received his M.S.E.E. degree in embedded system and electrical engineering from San Francisco State University. In 2010, he joined Maxim (later acquired by Analog Devices) and focused on multiphase buck management IC for Intel (consumer) definition and development. In 2017, Issac joined the Maxim Integrated Automotive Business Team. He is currently working on high current multiphase system and radar PIMIC for low noise applications.

Alexandr Ikriannikov is a fellow for the Communications and Cloud Power Team at Analog Devices. He received his Ph.D. degree in electrical engineering from Caltech in 2000, where he studied power electronics from Dr. Slobodan Ćuk. His graduate school projects ranged from power factor correction for AC-to-DC applications to 15 V to 400 V DC-to-DC for Mars rovers. After graduate school he joined Power Ten to redesign and optimize multi-KW AC-to-DC power supplies, then in 2001 joined Volterra Semiconductor concentrating on low voltage high current applications and coupled inductors. Volterra was acquired by Maxim Integrated in 2013, which is now part of Analog Devices. Currently, Alexandr is a senior member of IEEE. He holds more than 70 issued U.S. patents plus more pending and has authored multiple publications in the field of power electronics.